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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,693	02/05/2002	Cheng-Liang Huang	MICP0025USA	4545

27765 7590 10/27/2004

NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
PERVEEN, REHANA	
ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 10/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,693	HUANG, CHENG-LIANG	
	Examiner	Art Unit	
	Rehana Perveen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Where the specification identifies work done by another as "prior art," the subject matter so identified is treated as admitted prior art. In re Nomiya, 509 F.2d 566, 571, 184 USPQ 607, 611 (CCPA 1975) (holding applicant's labeling of two figures in the application drawings as "prior art" to be an admission that what was pictured was prior art relative to applicant's improvement).

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art, in view of Hoshino et al, Patent no. 6,804,300.

As to claim 1, applicant admits to a prior art computer comprising a processor for controlling operation of the computer (processor 12, figure 1), a card bus slot connected with the processor for connecting to a PCMCIA card (card bus slot 14, figure 1), a power supply for providing the PCMCIA card inserted into the card bus slot with electric power (power supply 16, figure 1), and a card bus controller connected with the processor for controlling the power supply and the PCMCIA card inserted into the card bus slot (card bus controller 18, figure 1).

However, applicant does not admit the computer further comprising a detection circuit connected with the card bus slot for detecting whether the PCMCIA card is inserted into the card bus slot, wherein when the detection circuit detects that the PCMCIA card has been inserted into the card bus slot, the card bus controller is turned on for making the power supply start to provide the PCMCIA card with electric power, and provides the PCMCIA card with the corresponding services according to a specification of the PCMCIA card for making the PCMCIA card operate correctly, and when the detection circuit detects that there is no PCMCIA card inserted into the card bus slot, the card bus controller is turned off for lowering power consumption.

Hoshino et al teach a personal computer comprising a detection circuit connected with a card bus slot for detecting whether a PCMCIA card is inserted into the card bus slot, wherein when the detection circuit detects that the PCMCIA card has been inserted into the card bus slot, a card bus controller is turned on for making a power supply start to provide the PCMCIA card with electric power, and provides the PCMCIA card with the corresponding services according to a specification of the PCMCIA card for making the PCMCIA card operate correctly, and when the detection circuit detects that there is no PCMCIA card inserted into the card bus slot, the card bus controller is turned off for lowering power consumption (col. 21 line 1 – col. 22 line 42).

It would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of the admitted prior art and Hoshino et al because both are commonly directed to the PCMCIA card support environment and Hoshino et al's detection of card insertion to determine whether to supply power would have enabled the improved system to achieve further efficiency by lowering the power consumption.

As to claim 2, applicant admits that the computer is a portable computer (portable computer 10, figure 1, applicant's disclosure, page 1).

As to claim 3, applicant admits that the power supply is capable of providing the PCMCIA card with different voltages, and the card bus controller controls the power supply for providing the PCMCIA card with an optimum voltage according to the specification of the PCMCIA card (applicant's disclosure, page 1).

As to claim 4, Hoshino et al teach the detection circuit generate a check signal for informing whether the PCMCIA card has been inserted into the card bus slot, and a processor turns on or turns off the card bus controller according to the check signal (col. 21 line 1 – col. 22 line 42).

Claims 5-8 are directed to the method of system claims 1-4. Applicant's admitted prior art and Hoshino et al, in combination, teach the system as set forth in claims 1-4.

Therefore, applicant's admitted prior art and Hoshino et al, in combination, also teach the method as set forth in claims 5-8.

Claims 1-8 are also rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art, in view of Evoy, Patent no. 6,062,480.

As to claim 1, applicant admits to a prior art computer comprising a processor for controlling operation of the computer (processor 12, figure 1), a card bus slot connected with the processor for connecting to a PCMCIA card (card bus slot 14, figure 1), a power supply for providing the PCMCIA card inserted into the card bus slot with electric power (power supply 16, figure 1), and a card bus controller connected with the processor for controlling the power supply and the PCMCIA card inserted into the card bus slot (card bus controller 18, figure 1).

However, applicant does not admit the computer further comprising a detection circuit connected with the card bus slot for detecting whether the PCMCIA card is inserted into the card bus slot, wherein when the detection circuit detects that the PCMCIA card has been inserted into the card bus slot, the card bus controller is turned on for making the power supply start to provide the PCMCIA card with electric power, and provides the PCMCIA card with the corresponding services according to a specification of the PCMCIA card for making the PCMCIA card operate correctly, and

when the detection circuit detects that there is no PCMCIA card inserted into the card bus slot, the card bus controller is turned off for lowering power consumption.

Evoy teaches a personal computer comprising a detection circuit connected with a card bus slot for detecting whether a PCMCIA card is inserted into the card bus slot, wherein when the detection circuit detects that the PCMCIA card has been inserted into the card bus slot, a card bus controller is turned on for making a power supply start to provide the PCMCIA card with electric power, and provides the PCMCIA card with the corresponding services according to a specification of the PCMCIA card for making the PCMCIA card operate correctly, and when the detection circuit detects that there is no PCMCIA card inserted into the card bus slot, the card bus controller is turned off for lowering power consumption (col. 3 line 25 – col. 4 line 24).

It would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of the admitted prior art and Evoy because both are commonly directed to the PCMCIA card support environment and Evoy's detection of card insertion to determine whether to supply power would have enabled the improved system to achieve further efficiency by lowering the power consumption.

As to claim 2, applicant admits that the computer is a portable computer (portable computer 10, figure 1, applicant's disclosure, page 1).

As to claim 3, applicant admits that the power supply is capable of providing the PCMCIA card with different voltages, and the card bus controller controls the power supply for providing the PCMCIA card with an optimum voltage according to the specification of the PCMCIA card (applicant's disclosure, page 1).

As to claim 4, Evoy teaches the detection circuit generate a check signal for informing whether the PCMCIA card has been inserted into the card bus slot, and a processor turns on or turns off the card bus controller according to the check signal (col. 3 line 25 – col. 4 line 24).

Claims 5-8 are directed to the method of system claims 1-4. Applicant's admitted prior art and Evoy, in combination, teach the system as set forth in claims 1-4. Therefore, applicant's admitted prior art and Evoy, in combination, also teach the method as set forth in claims 5-8.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rehana Perveen whose telephone number is 571-272-3676. The examiner can normally be reached on 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Primary Patent Examiner
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